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Reliability Analysis Of 1200 V SiC MOSFETs Under High Temperature And High Gate Voltage Step Stress Through Accelerated Lifetime Testing

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An experimental investigation of the reliability of two different 1200 V-rated planar and trench SiC MOSFETs was done, focusing on reliability and robustness differences between the two gate oxide technologies. In this work, we analyze this data, focusing primarily on the step-stress test design, where the gate voltage was increased with time, aiming to accelerate the testing time and investigate the acceleration as a function of voltage stress. Due to the limited data, a parametric approach using the Weibull distribution and the Eyring model is used. Different models for reliability under variable stress conditions and methods to identify significant differences in the lifetime of the two technologies under usage conditions are compared. Finally, some investigations into the design of future experiments are discussed.

In conclusion, the study aims to advance the analysis of typical step-stress testing approaches in the semiconductor industry. It shows how this provides a better understanding of the reliability and robustness differences in 1200 V-rated planar and trench SiC MOSFETs. The findings from this analysis can contribute to the advancement of reliability assessment methodologies for SiC power MOSFETs, providing valuable insights for developing and applying these technologies in various industrial sectors.