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Reliability Prediction Of Ultra High Performance Buffer For High Speed Applications

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Abstract

This study investigates the reliability prediction of an ultra-high-performance buffer for high-speed applications when neither field data nor lab data are available early in the design phase before prototype physical tests. Those digital buffers are used in test equipment for high-speed digital I/O (in mil/aero) applications. Such Reliability prediction analysis is based on MIL-HDBK-217 reliability prediction standard. It will be also shown how the derating is applied to increase the margin of safety between part design limits and applied stresses.

Keywords: reliability, prediction, standard.

1. Introduction

In the early stages of product design, it is often necessary to estimate the reliability of one or more design alternatives. Most reliability analysis tools require times to failure data, either at the component or at the system level, to estimate reliability. Standards based reliability prediction is a method to estimate the reliability of a product before test or field data are available.

Each component in the system is assumed to have a constant failure rate. Each Reliability Prediction standard includes mathematical formulas to calculate the failure rate of several components. These equations are built by analysing field data over a long period of time. Statistical analysis was then used to create the equations which best modelled the failure properties and characteristics of the data. MIL-HDBK-217 is very well known in military and commercial industries. It is probably the most internationally recognized empirical prediction method, by far (US Department of Defence (DoD) 1991).

Typically, the failure rate for each component is the base failure rate for that type of component modified by multiplying factors based on:

- physical characteristics such as size or rated voltage;
- application characteristics such as operating temperature or environment.

In today's competitive electronic products market, having higher reliability than competitors is one of the key factors for success. To obtain high product reliability, consideration of reliability issues should be integrated from the very beginning of the design phase. This leads to the concept of reliability prediction. Historically, this term has been used to denote the process of applying mathematical models and component data for the purpose of estimating the field reliability of a system before failure data are available for the system.
Once the prototype of a product is available, lab tests can be utilized to obtain more accurate reliability predictions.

2. Failure Rate Prediction

Empirical prediction methods are based on models developed from statistical curve fitting of historical failure data, which may have been collected in the field, in-house or from manufacturers. The *MIL*-HDBK-*217F* parts stress method provides constant failure rate *models* based on *curve-fitting* the *empirical* data obtained from field operation and testing. These methods tend to present good estimates of reliability for similar or slightly modified parts. Some parameters in the curve function can be modified by integrating engineering knowledge. The

assumption is made that system or equipment failure causes are inherently linked to components whose failures are independent of each other. There are many different empirical methods that have been created for specific applications. This standardization handbook was developed by the Department of Defence with the assistance of the military departments, federal agencies, and industry.

Let's perform a Reliability Prediction for an ultra-high-performance buffer for high-speed applications: A CMOS Buffer (laboratory application, case temperature 48 C, 75mW power dissipation, 28 C/W Junction Temperature) is procured with normal manufacturer's screening consisting of temperature cycling, constant acceleration, electrical testing, seal test and external visual inspection, in the sequence given. The component manufacturer also performs a B-level burn-in followed by electrical testing. All screens and tests are performed to the applicable MILSTD-883 screening method (US Department of Defence (DoD) 1991). The package is a 5 pin Non- Hermetic SMT. The device has been manufactured for several years and has 1 gate.

The type of model used for the CMOS Buffer is the following one:

$$\boldsymbol{\lambda p} = (C1 * \pi T + C2 * \pi E) * \pi Q * \pi L \quad (1)$$

Where:

- λp is the part failure rate;
- C1 Is the die complexity failure rate;
- πT Is the temperature factor;
- C2 is the Package failure rate;
- πE is the environment factor;
- πQ is the quality factor;
- πL is the learning factor.

Failure rate estimations are based on the Reliability Standard:
1) Die complexity failure rate.
CMOS Buffer has only 1 gate and , according to the standard, when:
No. Gates goes from 1 to 100 -> **C1 = 0.01**
It is shown in Figure 1.

Die Complexity Rate	**0.0100**
Technology	Comp Metal Oxide Semicon
Number of Gates	1

Fig. 1. The table of the Die Complexity Rate.

2) Temperature factor

Temperature factor (πT) is based on the device junction temperature:

$$\boldsymbol{\pi T} = 0.1\text{^}\left(\left(-\frac{Ea}{8.6x10^{-5}}\right)\left(\left(\frac{1}{Tj+273}\right)-\frac{1}{298}\right)\right) \quad (2)$$

Ea (activation energy) = 0.35 eV for the CMOS.
There are several methods for calculating the junction temperature:

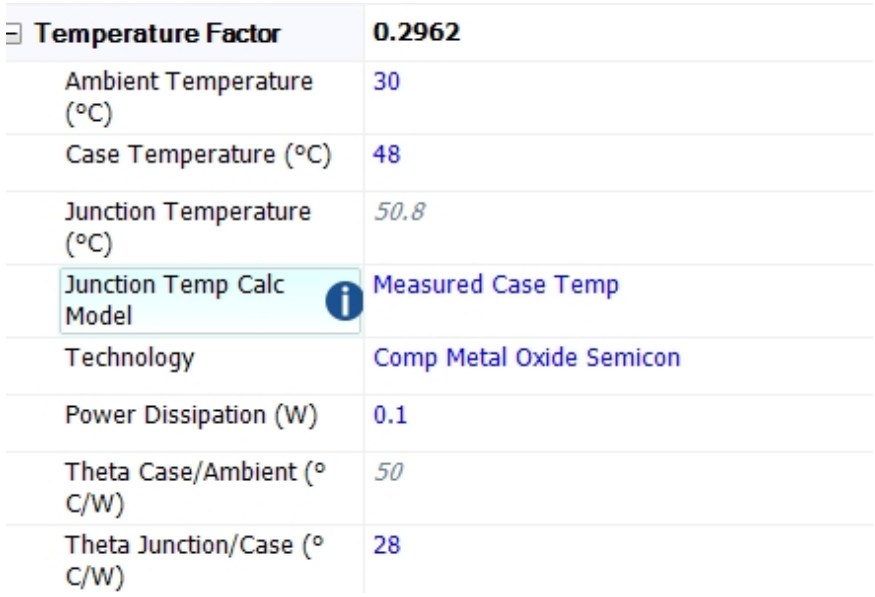
- Default Temperature Rise;
- Default Case Temperature and Theta Junction/Case;
- User Defined Junction Temperature;
- Unknown Power Dissipation;
- Measured Case Temperature;
- Full Model.

According to the available data, we choose the Default Case Temperature and Theta Junction/Case, using the following formula:

$$\mathbf{Tj} = Tcase + (Thermal\ resistance * Power\ dissipated) \quad (3)$$

$\mathbf{Tj} = 48°C + (28°C/W * 0.75W)$ -> $\boldsymbol{\pi T}$ **= 0.2962**

Temperature Factor calculation is shown in Figure 2



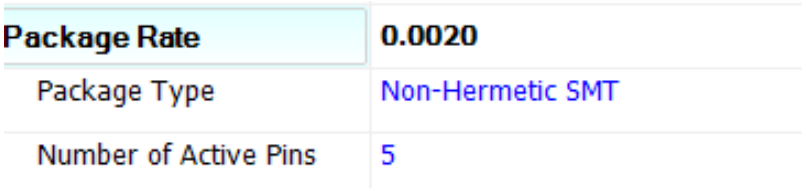
Temperature Factor	0.2962
Ambient Temperature (°C)	30
Case Temperature (°C)	48
Junction Temperature (°C)	*50.8*
Junction Temp Calc Model	Measured Case Temp
Technology	Comp Metal Oxide Semicon
Power Dissipation (W)	0.1
Theta Case/Ambient (° C/W)	*50*
Theta Junction/Case (° C/W)	28

Fig. 2. The table of the Temperature Factor.

3) Package failure rate

$$C2 = 3.6 * 10^{-4} * Np^{1.08} \quad (4)$$

The package is a 5 pin Non- Hermetic SMT
C2= 0.02
Package Rate calculation is shown in Figure 3



Package Rate	0.0020
Package Type	Non-Hermetic SMT
Number of Active Pins	5

Fig. 3. The table of the Package Rate.

4) Environment factor

According to the standard:
Nonmobile, temperature and humidity-controlled environments readily accessible to maintenance; includes laboratory instruments and test equipment, medical electronic equipment, business and scientific computer complexes, and missiles and support equipment in ground silos -> **πE** = 0.5.
Moderately controlled environments such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings; includes permanent installation of air traffic ¡c control radar and communications facilities -> πE = 2.
Equipment installed on wheeled or tracked vehicles and equipment manually transported; includes tactical missile ground support equipment, mobile communication equipment, tactical fire direction systems, handheld communications equipment, laser designations and range finders -> **πE** = 4.
The CMOS Buffer is used for some laboratory application, therefore **πE =** 0.5.
Environment Factor is shown in Figure 4

Environment Factor	0.5000
Environment	Ground, benign

Fig. 4. The table of the Environment Factor.

5) Quality factor

$\pi Q = 2 + (87/\sum \text{Points Valuations})$ (5)

Where:

Group 1: TM 1010 (Temperature Cycle, Cond B minimum) and TM 2001 (Constant Acceleration Cond B minimum) and TM 5004 (Final Electrical @ Temp Extremes) and TM 1014 (Seal Test, Cond A, B, or C) and TM 2009 (External Visual) -> Points Evaluations = 50.
Group 2: TM 1010 (Temperature Cycle, Cond B Minimum) or TM 2001 (Constant' Acceleration, Cond B Minimum) TM 5004 (or 5008 for Hybrids) (Final Electricals @ Temp Extremes) and TM 1014 (Seal Test, Cond A, B, or C) and TM 2009 (External Visual)-> Point Evaluations = 37 Points.
Group 3: Pre-Bum in Electricals TM 1015 (Burn-in B-LeveVS-Level) and TM 5004 (of 5008 for Hybrids) (Post Bum-in Electricals @ Temp Extremes) -> Points Evaluations = 30 Points.
CMOS Buffer is procured with normal manufacturer's screening consisting of temperature cycling, constant acceleration, electrical testing, seal test and external visual inspection, in the sequence given. The component manufacturer also performs a B-level burn-in followed by electrical testing. Therefore, Point Valuations = (50 Points + 30 Points) = 80 Points.

$\boldsymbol{\pi Q} = 2 + \left(\frac{87}{50+30}\right)$

$\boldsymbol{\pi Q} = 3.08$

Quality Factor calcolation is shown in Figure 5

Quality Factor	3.0875
Quality, Microelectronics	Use Point Valuation
Total Point Valuation	80

Fig. 5. The table of the Quality Factor.

6) Learning factor

When Number of years since introduction to field use is smaller or equal than 1 -> $\boldsymbol{\pi L} = 10$.
When Number of years since introduction to field use is bigger than 1 and smaller than 3 -> $\boldsymbol{\pi L} = 10 * T^{-2.1}$.
When Number of years since introduction to field use is bigger than 3 -> $\boldsymbol{\pi L} = 1$.
As the CMOS buffer has been manufactured for several years, - > $\boldsymbol{\pi L} = 1$.
Learning Factor calculation is shown in Figure 6

Learning Factor	1.0000
Number of Years in Production	2

Fig. 6. The table of the Learning Factor.

Therefore, the part failure rate, $\boldsymbol{\lambda p} = (0.01 * 0.2962 + 0.002 * 0.5) * 3.08 * 1 = (0.002962 + 0.001) * 3.08 = 0.0039 * 3.08 = 0.012$ -> $\boldsymbol{\lambda p} = 0.0123$

Failure Rate calculation is shown in Figure 7

Fig. 7. The table of Failure Rate Part Item.

3. Derating Analysis

Most equipment failures are precipitated by stress (European Cooperation for Space Standardization 2006). When the applied stress exceeds the inherent strength of the part, either a serious degradation or a failure will occur. To assure reliability, the equipment must be designed to endure stress over time without failure. In addition, design stress parameters must be identified and controlled, while parts and materials that can withstand these stresses must be selected. Derating standards are used to help you select and use parts and materials so that the applied stress is less than rated for a specific application (U.S. Naval Air Systems Command 1976)**.** Derating is a technique usually employed in electrical power and electronic devices, wherein the devices are operated at less than their rated maximum power dissipation, considering the case/body temperature, the ambient temperature and the type of cooling mechanism used (U.S. National Aeronautics and Space Administration 1994). By applying derating in an electrical or electronic component, its degradation rate is reduced. The reliability and life expectancy are improved. Intuitively, if a component or system is operated under its design limit, it will be more reliable than if it is operated at or above the design limit. Several derating guidelines have been issued. For this example I am using the MIL-STD-1547 that was published by the Department of Defense and it is targeted to aid in the design, development and fabrication of electronic systems with long life and/or high reliability requirements (U.S. Department of Defense (DoD) 1998).

The Derating page displays a plot of the component's derating curves provided by the derating standard that we are working with (Naval Sea Systems Command 1991). The nominal case curve is displayed in green, and the worst-case curve is displayed in red. The blue dot on the plot shows the component's working temperature and stress ratio. The location of the blue dot on the plot indicates the component's derating status:

- If the blue dot is within the nominal curve, the component is not stressed.
- If the blue dot is between the nominal and worst-case curves, then the component exceeds nominal values, but is not overstressed.
- If the blue dot is outside the worst-case curve, the component is overstressed.

Power Stress vs Temperature plot is shown in Figure 8 and it is based on MIL-STD-1547 standard.

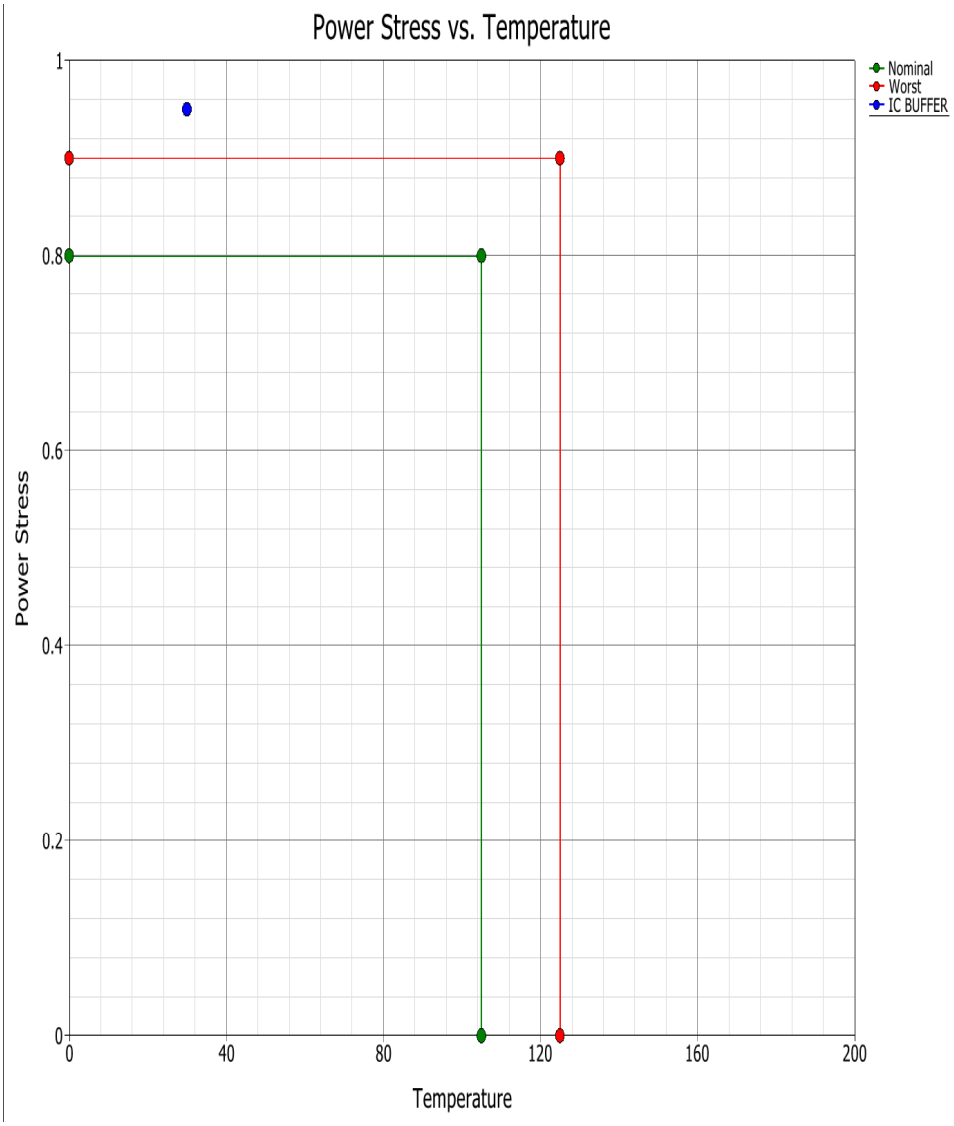


Fig. 8. The plot of the Power stress vs Temperature above design limit.

As we can notice, when the Power Stress = 0.9 and Ambient Temperature = 30 ℃, the blue dot is outside the worst-case curve, so the item is overstressed.

To operate under the design limit and the nominal curve, the Power Stress needs to be lower.

Reviewed Power Stress vs Temperature plot is shown in Figure 9 and it is based on MIL-STD-1547 standard.

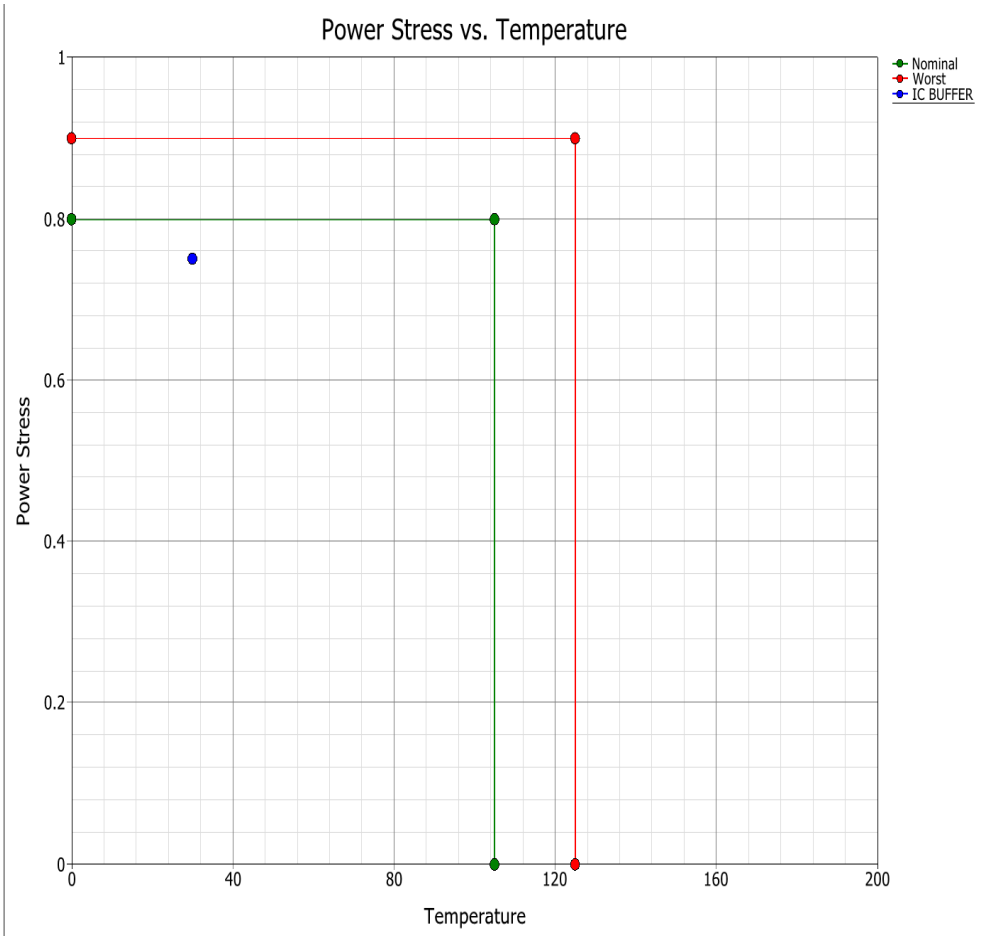


Fig. 9. The plot of the Power stress vs Temperature below nominal curve.

From the plot above, we can notice that when the Power Stress = 0.75 and the Ambient Temperature = 30 ℃, the blue dot is within the nominal curve, so the component is not stressed.

4. Conclusion

This study investigated the reliability prediction of an ultra-high-performance buffer for high-speed applications when neither field data nor lab data are available early in the design phase before prototype physical tests. Such Reliability prediction analysis is based on one of the major published standards, MIL-HDBK-217F. The following factors have been calculated.

1) C1 Is the die complexity failure rate.
2) πT Is the temperature factor.
3) C2 is the Package failure rate.
4) πE is the environment factor.
5) πQ is the quality factor.
6) πL is the learning factor.

and finally, the failure rate for the ultra-high-performance buffer for high-speed applications is provided based on formulas included in such standard (1).

Further investigation showed that, according to the derating standard (US Department of Defence (DoD) 1998), a certain value of power stress needs to be decrease in order not to exceeds the inherent strength of the part.

Acknowledgement

The paper presents the results of ultra-high-performance buffer for high-speed applications failure rate calculation.

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