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Thermal Cycling Life Prediction Of TSV Microstructure Based On Accelerated Test

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Abstract

Three-dimensional integrated packaging technology with through silicon via (TSV) and stack as typical features is the key technology to surpass Moore's Law, but its reliability in service has not been completely solved. As the microstructure of TSV is composed of multiple materials and multiple interfaces, there is thermal mismatch phenomenon, so the internal stress and strain of the structure is very sensitive to temperature change. Based on the TSV test chip specially designed for multi-stress reliability test and the accelerated test method, the life prediction of TSV microstructure under thermal cycling conditions is carried out in this paper, which can provide an important reference for the reliability evaluation and optimization design of three-dimensional package chips based on TSV.

Keywords: through silicon via TSV, accelerated test, thermal cycling, life prediction

1. Introduction

Using TSV as the energy and signal path, vertically stacked 3D integrated chips break through the performance limitations on the two-dimensional chip plane, and have the advantages of lower power consumption, higher bandwidth, lower latency, and smaller size. Intel, AMD, and other major chip companies regard 3D packaging products as the key to the next generation of chip competition. Before any new product can be brought to market, reliability issues must first be addressed. However, the reliability test and evaluation of TSV microstructures are still lacking, especially the reliability problems in service need to be further studied (Fan et al., 2019, 2020a, 2020b, 2022; Hou et al., 2023).

Due to the small scale of TSV microstructure, it is necessary to design a dedicated chip for testing, and it is difficult to monitor its failure and degradation in situ and in real time. Therefore, there are few reports on the reliability test and life prediction of TSV microstructure, and the existing studies focus on the load conditions of electrical and thermal stress. Khan (Khan et al., 2010) designed a stacked package chip based on TSV and conducted tests using daisy chain resistance as a monitoring parameter. It was found that the TSV structure failed within 500 thermal cycles, while the solder joint did not fail within 2000 cycles. Okoro et al. (Okoro et al., 2014) took Daisy chain resistance decline as the performance degradation parameter of TSV, conducted experimental research on it under thermal cycling load, and analyzed the influence of different damage forms on structural resistance based on electrical model.

Chung Chung et al., 2016) designed three TSV chains (Kelvin chain, through hole chain and metal electrode chain), conducted electrical stress tests on them based on JEDEC standard, and determined that the life data obeyed Weibull distribution. Finally, the failure analysis of the structures was carried out using optical microscopy and scanning electron microscopy. Banijamali (Banijamali et al., 2011a, 2011b, 2012, 2015) investigated the influence of different structural designs and material parameters on structural reliability of the TSV interposer with high aspect ratio Cu-TSV and very small bumps by in-situ reliability test (resistance data) under temperature load, predicted the fatigue life of the micro-bumps, and optimized the structure by DoE method.

Croes Croes et al., 2012) summarized IMEC's research results on TSV reliability. Using transistor as stress sensor and its bias as parameter index, the influence of heat storage and thermal shock on structural reliability is studied. Dixit Dixit et al., 2013) designed a partially filled conical through-silicon hole and conducted electrical and thermal stress tests on it, pointing out that manufacturing defects are the main cause of structural failure. Lwo et al. (Lwo et al., 2012, 2013, 2014, 2016a, 2016b) conducted an experimental study on the reliability of TSV structure under the current bias, thermal aging, thermal cycling, and the combined stress of wet and thermal cycling, and took the resistance change of 10% as the failure criterion to obtain the structural life test data. Assuming the life obeys Weibull distribution, distribution parameter estimation and life analysis were conducted based on the test data. It is found that the current bias is the most important factor affecting the reliability of TSV structure, followed by the wet and thermal cycling. Chan et al. (Chan et al., 2016, 2017a, 2017b, 2018) used electrical testing methods and physical failure analysis (PFA) methods to conduct experimental research on the degradation of isolation layer and insulation layer in TSV structure under electrical stress, temperature cycling and high-temperature storage stress, and found that the migration of copper over the degraded isolation layer to the dielectric layer was the main cause of structural failure. Huang et al. (Huang et al., 2015, 2016) conducted an experimental study on the reliability of air gap insulation TSV under thermal, electrical, drop, vibration, high humidity, and other stresses. Raman spectroscopy was used to measure the residual stress of silicon substrate and analyze the failure mechanism. In addition, JEDEC published the TSV test standard JEP158 JEDEC Association, 2009), which provided guidance and suggestions for reliability testing and failure analysis of TSV.

The main research methods mentioned above are as follows: First, a dedicated test chip is designed, then structural resistance is used to characterize TSV structural degradation, and microscopic characterization is used to assist failure analysis. However, most of the existing studies focus on the single stress, which is to determine the failure mode of the structure, and the quantitative analysis of the life of the TSV structure is still lacking.

In the author's previous report Fan et al., 2022), we designed a TSV chip that can carry out multi-stress reliability tests, carried out performance degradation tests under thermal cycling, electrical stress and vibration stress, and analyzed the failure mode. Based on the TSV test chip, the life of TSV microstructure under thermal cycling load is quantitatively predicted in this paper. Due to the long life of TSV microstructure under thermal cycling, the test cycle and cost under use stress are large, so it is necessary to take accelerated test.

This paper first introduced the test platform and test device, then designed the accelerated thermal cycling test scheme. The accelerated life test was carried out according to the test scheme to obtain the test data, and then the distribution fitting of the test data was given. Based on the life test data, an accelerated test model was established, and the consistency of failure mechanism was checked. Finally, the life of TSV microstructure under thermal cycling was predicted. The research methods and conclusions of this paper can provide method support and theoretical reference for reliability test, evaluation and optimization design of three-dimensional package chip based on TSV.

2. Test platform and test device

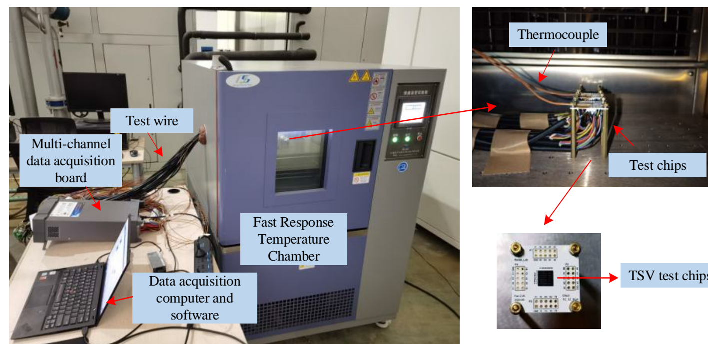

Fig. 1. Thermal cycling test platform and test device.

Thermal cycling stress is the most common stress in the service process of TSV structures. Based on the TSV multi-stress test chip (Fan et al., 2022) designed by the author's laboratory, the thermal cycling test platform and test device are designed, as shown in Figure 1, which consists of a rapid response temperature chamber and a

multi-channel digital data acquisition system. The digital data acquisition system can monitor and collect the chip signal and temperature in real time through the chip signal test line and thermocouple.

3. Thermal cycling acceleration test scheme design

Based on the initial test, the samples with large initial resistance (damaged) are removed, and the thermal cycling acceleration test was carried out with the resistance change of 20% as the failure criterion. With thermal cycling temperature difference as accelerating stress and reference to JEDEC JESD22-A104F test standard (JEDEC Association, 2014), the thermal cycling acceleration test scheme was designed as shown in Table 1. The sample size under each test section is greater than 12 (qualified samples are screened according to the initial test, so the qualified sample size on each test chip is different). The test of each profile is censored according to the corresponding number of thermal cycles determined by the failure condition of the sample.

Table 1. Thermal cycle acceleration test scheme.

Test number	Thermal cycling temperature	Thermal cycling temperature change	Test ID	Sample size	Reference standard
1	−40-150℃	190℃	KC-TC-1	39	JEDEC JESD22-A104F Condition M
2	−25-125℃	150℃	KC-TC-2	19	JEDEC JESD22-A104F Condition R
33	0-100℃	100℃	KC-TC-3	22	JEDEC JESD22-A104F Condition J

4. Thermal cycling acceleration test life data and distribution fitting

According to the above test scheme, the test was carried out with 300, 512 and 1847 thermal cycles censore under the three test profiles, and the test time was about 12.5, 21.3 and 77 days, respectively. The test data were shown in Figure 2 and Table 2, and the numbers in brackets after the life data in Table 2 were the sample number of the same data point.

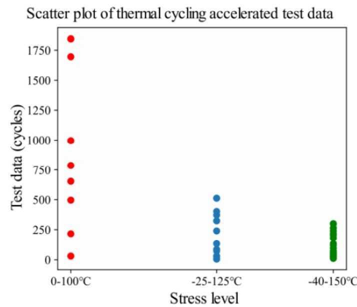

Fig. 2. Thermal cycling acceleration test data.

Table 2. Thermal cycling acceleration test data.

Thermal cycling(℃)	Temperature change	Number of failure samples	Complete life data	Number of censored samples	Censored life data
0-100	100	7	30，216，496，656，786，996，1697	15	1847(15)
−25-125	150	14	6(3)，30(2)，72，84，132，240，324(3)，372，402	5	512(5)
−40-150	190	34	12(3)，24(10)，36(3)，48(3)，60(3)，72(2)，96，120，132，180，204，216，240，264(3)	5	300(5)

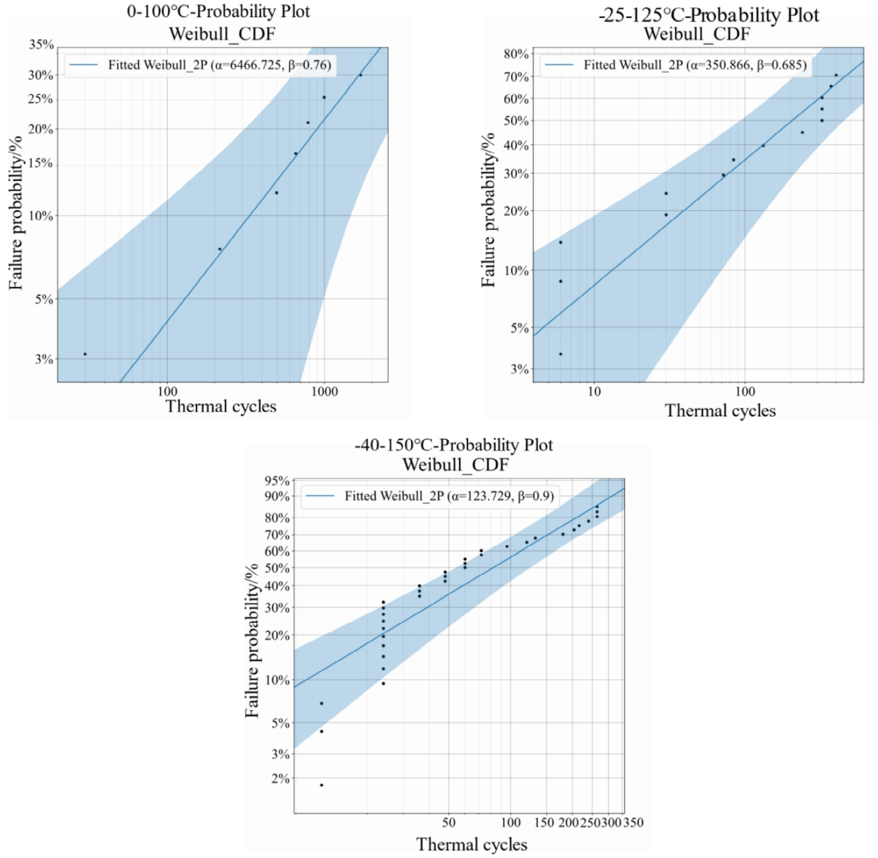

Fig. 3. Distribution fitting of censored life data.

The distribution fitting of test data under each stress level was carried out, and after Pearson Chi-square hypothesis test, it was determined that the life data under each stress level obeyed the two-parameter Weibull distribution with 95% confidence. The distribution parameters and probability plot are shown in Figure 3. It can be seen from the figure that the more complete life data, the narrower the confidence interval of the fitting distribution.

5. Thermal cycling acceleration test model and failure mechanism consistency check

After the life distribution of each stress level was determined, the accelerated test model was constructed, and the failure mechanism consistency was checked for all the data under all stress levels. The failure mechanism of TSV structure under thermal cycling is high cycle fatigue and crack propagation, and the life-stress relationship is a power law relationship in the shape of $L = a \cdot S^n$. Therefore, it is clear that when the life of TSV structure under the action of thermal cycling obeys the two-parameter Weibull distribution, its acceleration model is Weibull - power law acceleration model (in the form of failure probability density function):

$$f(t,S) = \frac{\beta t^{\beta-1}}{(a \cdot S^n)^\beta} \cdot exp\left(-\left(\frac{t}{a \cdot S^n}\right)^\beta\right) \quad (1)$$

where the Weibull scale parameter α is replaced by the life-stress relation model, i.e. $\alpha = L(S) = a \cdot S^n$, β is the Weibull shape parameter, and a and n are the life-stress model parameters. Then its reliability function, cumulative failure distribution function and failure rate function are:

$$R(t) = exp\left(-\left(\frac{t}{a \cdot S^n}\right)^{\beta}\right) \tag{2}$$

$$F(t) = 1 - exp\left(-\left(\frac{t}{a \cdot S^n}\right)^{\beta}\right) \tag{3}$$

$$h(t) = \frac{\beta}{a \cdot S^n}\left(\frac{t}{a \cdot S^n}\right)^{\beta-1} \tag{4}$$

When the test data is composed of complete life data and right censored life data, the logarithmic likelihood function is:

$$ln(l) = \sum_{i=1}^{N_c} n_i \cdot ln[f(t_i, S_i; \beta, a, n)] + \sum_{j=1}^{N_r} n_j \cdot ln[1 - F(t_j, S_j; \beta, a, n)]$$
$$= \sum_{i=1}^{N_c} n_i \cdot ln\left[\frac{\beta t_i^{\beta-1}}{(a \cdot S_i^{\,n})^{\beta}} \cdot exp\left(-\left(\frac{t_i}{a \cdot S_i^{\,n}}\right)^{\beta}\right)\right] + \sum_{j=1}^{N_r} n_j \cdot ln\left[exp\left(-\left(\frac{t_j}{a \cdot S_j^{\,n}}\right)^{\beta}\right)\right] \tag{5}$$

Let (5) satisfy the equation:

$$\frac{\partial\, ln(l)}{\partial \theta_M} = 0 \tag{6}$$

Estimates of all model parameters at all stress levels can be obtained from the test data, as shown in Table 3.

Table 3. Thermal cycling acceleration test model parameters.

Model parameters	Point estimate	Standard deviation	Lower confidence limit 95%	Upper confidence limit 95%
a	4.66218e8	3.80505e8	9.4163e7	2.30833e9
n	-2.77539	0.16943	-3.10746	-2.44331
β	0.749199	0.0891482	0.593351	0.945982

Table 4. Thermal cycling accelerated test failure mechanism consistency test.

Stress level	Original scale parameter α_i	Original shape parameter β_i	Acceleration model scale parameters α	Acceleration model shape parameters β	Rate of change of shape parameters	Acceleration ratio
190	123.74	0.899534	220.884	0.749199	-16.71%	40.656
150	351.201	0.684885	425.689	0.749199	+9.39%	21.0958
100	6478.67	0.759212	1311.64	0.749199	-1.32%	6.8466

The life distribution model parameters under each stress level and those obtained by maximum likelihood estimation are shown in Table 4. The consistency of failure mechanism can be tested by comparing the change of shape parameters in the model (the change is less than 50%) (Reid, 2022).

It can be seen from Table 4 that the relative change of shape parameters in the accelerated test model is less than 20% compared with the life distribution shape parameters under each stress level (far less than the threshold of 50%). Therefore, it can be determined that the failure mechanism of TSV structure under the three thermal cycling accelerated stress levels is consistent, and the accelerated test model is applicable.

6. Life prediction of TSV structure under thermal cycling

Based on the consistency of accelerated failure mechanism, the reliability function and cumulative failure distribution function of TSV structure under thermal cycling stress can be obtained from Table 3 and Table 4 as follows:

$$R(t, S_i) = exp\left(-\left(\frac{t}{4.66218\times10^{8} \cdot S_i^{\,-2.77539}}\right)^{0.749199}\right) \tag{7}$$

$$F(t, S_i) = 1 - exp\left(-\left(\frac{t}{4.66218\times10^{8} \cdot S_i^{\,-2.77539}}\right)^{0.749199}\right) \tag{8}$$

Its curve is shown in Figure 4 under the use stress level (let the chip operating temperature range be 50˚C).

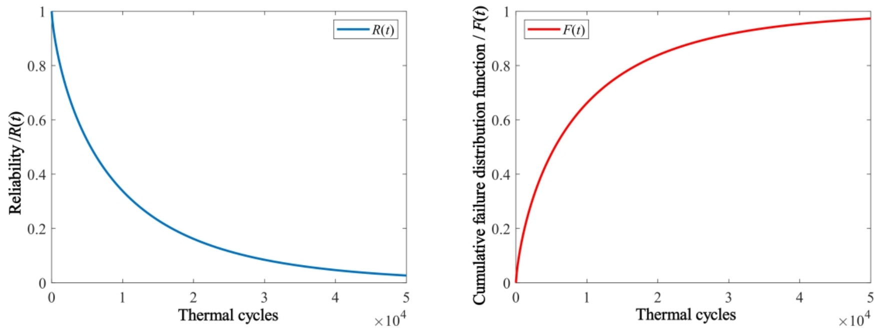

Fig. 4. (a). Curve of reliability function; (b). Curve of cumulative failure distribution.

Its average life under service stress is:

$$\mu = \alpha \cdot \Gamma(1 + \frac{1}{\beta}) = a \cdot S_{use}^{n} \cdot \Gamma(1 + \frac{1}{\beta}) \quad (9)$$

According to the above equation, the life under ues stess can be predicted by "extrapolation", where $\Gamma(\cdot)$ is the gamma function. The probability plot and life-stress relationship under various stress levels are shown in Figure 5.

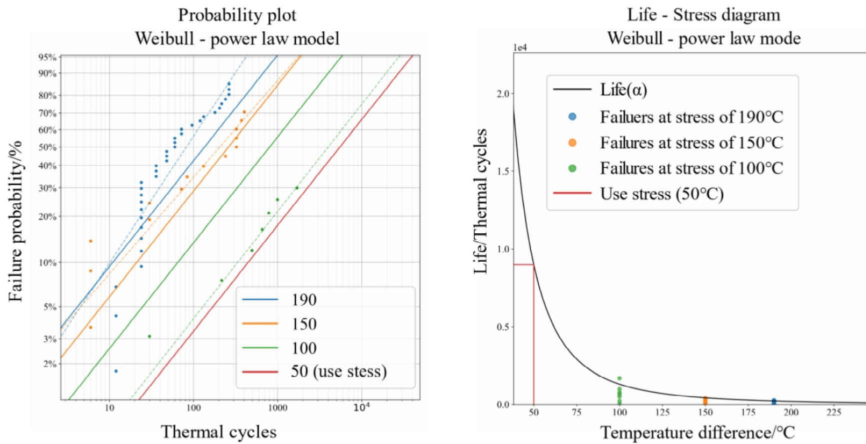

Fig. 5. (a) Probability plot for each stress level; (b) Life-stress diagram.

As shown in Figure 5, when the thermal cycling temperature range of the stress is 50˚C it can be obtained that the average working life of the TSV structure under the thermal cycling stress is 10701.7 cycles, and the maximum acceleration ratio is 40.7. Assuming that the TSV structure carries 10 thermal cycles per day, its lifetime under the single stress of the thermal cycling is 2.9320 years at the 95% confidence level. Assuming that the TSV structure carries 2 thermal cycles per day, its lifetime under the single stress of the thermal cycliing is 14.6599 years at the 95% confidence level.

7. Conclusions

Based on TSV reliability test chip and accelerated test method, the life prediction of TSV microstructure is quantified. The acceleration ratio reaches 40.7, which proves the effectiveness of the test chip. The test method and model in this paper can provide the basis and reference for reliability evaluation and optimization design of 3D package chip based on TSV.

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